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DATE: Tuesday, October 19, 2004

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	DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L12	l4 same (continu$7 near5 clock$4)	47
☐	L11	l8 same (continu$7 near5 clock$4)	1
☐	L10	l8 same (fail$4 or safe$4)	0
☐	L9	((system or main) near2 clock near2 generat$4) with (local near2 clock near2 generat$4)	43
☐	L8	((system or main) near2 clock near2 generat$4) same (local near2 clock near2 generat$4)	59
☐	L7	L4 same (local$4 near2 clock)	14
☐	L6	L4 and ((local$4 near2 clock) near5 continu$9)	1
☐	L5	L4 same ((local$4 near2 clock) near5 continu$9)	0
☐	L4	(system adj clock) near5 (fail$4 or error or shut$5 or stop$4)	1112
☐	L3	(system adj clock) with (fail$4 or error or shut$5 or stop$4)	2010
☐	L2	L1 same (fail$4 or error or shut$5 or stop$4)	131
☐	L1	(local$9 near2 clock) same (system near2 clock)	832

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L11: Entry 1 of 1 File: USPT Dec 26, 1995

DOCUMENT-IDENTIFIER: US 5479648 A
TITLE: Method and apparatus for switching clock signals in a fault-tolerant computer system

Detailed Description Text (13):
Briefly, the multiplexer circuits include a first system multiplexer (SYS MUX) 600 configured to select between system clock pulses generated by the system clock unit 120 and logical ground. Similarly, a second local multiplexer (LOC MUX) 700 is configured to select between local clock pulses generated by the local clock unit 225 and logical ground. A third control multiplexer (CTL MUX) 800 is arranged to receive the outputs of SYS MUX 600 over a first set of input lines and the outputs of LOC MUX 700 over a second set of input lines. Advantageously, as described further herein, SYS MUX 600 and LOC MUX 700 are configured such that either system or local clock signals are constantly present at the outputs of these multiplexers, while CTL MUX 800 is configured to switch between the clock signals propagating over these sets of input lines in a manner that provides a substantially continuous stream of output clock pulses to selected components of the fault-tolerant system 100.

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L13: Entry 10 of 21 File: USPT Jun 14, 1994

DOCUMENT-IDENTIFIER: US 5321698 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for providing retry coverage in multi-process computer environment

Detailed Description Text (12):
The error reports from detectors 181 and 182 also go to the recovery control platform (ReCoP) 160. ReCoP 160 is independently clocked as indicated at 161 and thus it continues to operate even after pulses from system clock generator 110 are turned off by shut-off mechanism 184.

Detailed Description Text (24):
The retry control platform 160 then sends a clock start command to shut-off mechanism 184 to restart the supply of clock pulses from generator 110 to the IU, EU, and MMU. The error-infected process is retried from its start point while other processes within computer system 100 continue uninterrupted. (While system clocks are off they do nothing. After system clocks are restarted, they continue as if clock stoppage never occurred.)

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